

What is claimed is:

1. A method for fabricating a semiconductor device, comprising:
2 forming a dielectric layer overlaying a semiconductor substrate;
3 forming an opening in the dielectric layer;
4 embedding copper or copper alloy into the opening;
5 forming a silicon layer on the copper or copper alloy by sputtering; and
6 reacting the silicon layer with the underlying copper or copper alloy to form a
7 copper silicide layer capping the surface of the copper or copper alloy.

1. The method as claimed in claim 1, wherein the dielectric layer
2 comprises a low-k material having k value less than 3.2.

1. The method as claimed in claim 1, wherein the dielectric layer
2 comprises organic low-k material, CVD low-k material, a combination of organic
3 low-k material and CVD low-k material, carbon-containing silicon oxide, nitrogen-
4 containing silicon oxide, FSG, SiC, SiOC or SiOCN.

1. The method as claimed in claim 1, wherein the width of the opening is
2 less than 900Å.

1. The method as claimed in claim 1, wherein the thickness of the
2 embedded copper or copper alloy is less than 4000Å.

1. The method as claimed in claim 1, wherein the silicon layer comprises
2 amorphous silicon.

1 7. The method as claimed in claim 2, wherein the thickness of the silicon
2 layer is 50 to 500Å.

1 8. The method as claimed in claim 1, wherein the copper or copper alloy
2 is formed by the steps of:

3 depositing a copper seed layer in the opening; and
4 electro-chemical plating or electroless plating the copper or copper alloy on
5 the copper seed layer.

1 9. The method as claimed in claim 1, wherein the copper or copper alloy
2 is formed by chemical vapor deposition.

1 10. The method as claimed in claim 1, wherein the copper silicide layer is
2 formed by subjecting the semiconductor substrate to an inert gas-containing ambience
3 at a temperature of about 150 degrees C. to about 450 degrees C.

1 11. The method as claimed in claim 1, further comprising the steps of:
2 removing un-reacted portions of the silicon layer; and
3 forming a diffusion barrier layer overlaying the copper silicide.

1 12. The method as claimed in claim 11, wherein the diffusion barrier layer
2 comprises silicon-rich oxide, SiN, SiC, SiOC, SiOCN, carbon-containing silicon
3 oxide or nitrogen-containing silicon oxide.

1 13. The method as claimed in claim 11, further comprising a step of:
2 forming an etch-stop layer overlaying the diffusion barrier layer.

1 14. The method as claimed in claim 13, wherein the etch-stop layer
2 comprises silicon-rich oxide, SiC, SiOC, SiON, SiOCN, carbon-containing silicon
3 oxide or nitrogen-containing silicon oxide.

1 15. A method for fabricating a semiconductor device, comprising:
2 forming a dielectric layer overlaying a semiconductor substrate;
3 forming an opening in the dielectric layer;
4 embedding copper or copper alloy into the opening;
5 forming a silicon layer on the copper or copper alloy by chemical vapor
6 deposition; and
7 reacting the silicon layer with the underlying copper or copper alloy to form a
8 copper silicide layer capping the surface of the copper or copper alloy.

1 16. The method as claimed in claim 15, wherein the dielectric layer
2 comprises a low-k material having k value less than 3.2.

1 17. The method as claimed in claim 15, wherein the dielectric layer
2 comprises an organic low-k material, a CVD low-k material, a combination of organic
3 low-k material and CVD low-k material, carbon-containing silicon oxide, nitrogen-
4 containing silicon oxide, FSG, SiC, SiOC or SiOCN.

1 18. The method as claimed in claim 15, wherein the width of the opening
2 is less than 900Å.

1 19. The method as claimed in claim 15, wherein the thickness of the
2 embedded copper or copper alloy is less than 4000Å.

1 20. The method as claimed in claim 15, wherein the chemical vapor
2 deposition is plasma-enhanced chemical vapor deposition.

1 21. The method as claimed in claim 15, wherein the silicon layer
2 comprises amorphous silicon.

22. The method as claimed in claim 15, wherein the thickness of the
silicon layer is about 50 to 500Å.

5 23. The method as claimed in claim 15, wherein the copper or copper alloy
is formed by the steps of:

depositing a copper seed layer in the opening; and
electro-chemical plating or electroless plating the copper or copper alloy on
the copper seed layer.

1 24. The method as claimed in claim 15, wherein the copper or copper alloy
2 is formed by chemical vapor deposition.

1 25. The method as claimed in claim 15, wherein the copper silicide layer is
2 formed by subjecting the semiconductor substrate to an inert gas-containing ambience
3 at a temperature of about 150 degrees C. to about 450 degrees C.

1 26. The method as claimed in claim 15, further comprising the steps of:
2 removing un-reacted portions of the silicon layer; and
3 forming a diffusion barrier layer overlaying the copper silicide.

1 27. The method as claimed in claim 26, wherein the diffusion barrier layer
2 comprises silicon-rich oxide, SiN, SiC, SiOC, SiOCN, carbon-containing silicon
3 oxide, or nitrogen-containing silicon oxide.

1 28. The method as claimed in claim 26, further comprising a step of:
2 forming an etch-stop layer overlaying the diffusion barrier layer.

1 29. The method as claimed in claim 28, wherein the etch-stop layer
2 comprises silicon-rich oxide, SiC, SiOC, SiON, SiOCN, carbon-containing silicon
3 oxide or nitrogen-containing silicon oxide.